Hex Inverter (Open Drain)

General Description

The MM54HCT05/MM74HCT05 are logic functions fabricated by using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are also input-output characteristically and pin-out compatible with standard DM54LS/DM74LS logic families. The MM54HCT05/MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

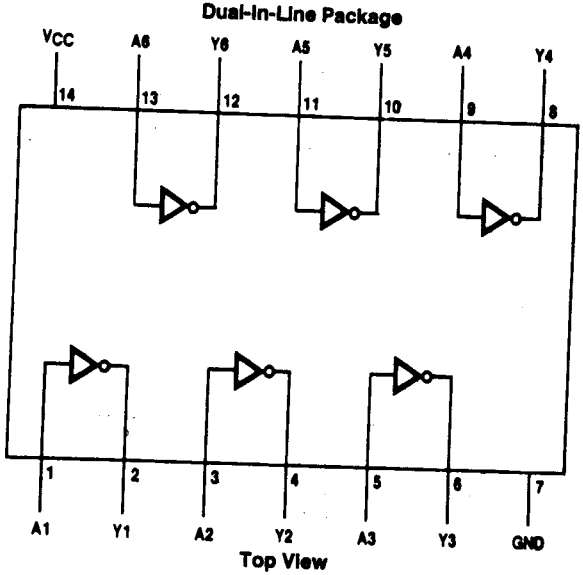
MM54HCT/MM74HCT devices are intended
tween TTL and NMOS components and
devices. These parts are also plug-in repla
TTL devices and can be used to reduce pow
in existing designs.

Features

- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fanout of 10 LS-TTL loads
- Typical propagation delays:
  t_{PLH} (with 1 kΩ resistor) 10 ns
  t_{PHL} (with 1 kΩ resistor) 8 ns

Connection Diagram

Dual-In-Line Package

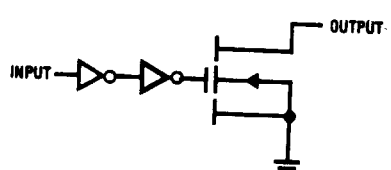


Top View

TL/F/5358–1

Order Number MM54HCT05J or MM74HCT05J, N
See NS Package J14A or N14A

Logic Diagram



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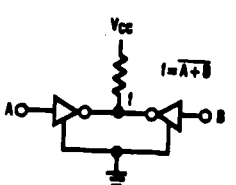
Typical Application



Note: Can be extended to more than 2 inputs.

DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

MM54HCT	−55
Input Rise or Fall Times (t_r, t_f)	

DC Electrical Characteristics (V_{CC} = 5V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40 to 85°C	5 T_A = −
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, R_L = 1 kΩ $\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN} = V_{IH} or VIL, V_{OUT} = V_{CC}		0.5	5.0	
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA		2.0	20	
		V_{IN} = 2.4V or 0.5V (Note 4)				

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

t_{PHL}	Maximum Propagation Delay	$R_L = 1\ k\Omega$	8	15	ns
t_{PLH}	Maximum Propagation Delay	$R_L = 1\ k\Omega$	9	16	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specifie

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$		54HCT $T_A = -55$ to $125°C$
			Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay	$R_L = 1\ k\Omega$	10	22	28	33
t_{PLH}	Maximum Propagation Delay	$R_L = 1\ k\Omega$	12	20	25	30
t_{THL}	Maximum Output Fall Time		10	15	19	22
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) $R_L = \infty$		20		
C_{IN}	Maximum Input Capacitance			5	10	10

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C$